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Attorneys for Plaintiff
IMPINJ, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

IMPINJ, INC., a Delaware corporation,

Plaintiff,

v.

NXP USA, INC., a Delaware corporation,

Defendant.

Case No. 19-cv-03161-YGR

SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

JURY TRIAL DEMANDED

Plaintiff Impinj, Inc. ("Impinj"), for its Second Amended Complaint, alleges as follows:

NATURE OF THE CASE

1. This is a complex patent infringement action arising from Defendant's copying of Impinj's patented innovations, its infringement of multiple patents owned by Impinj, its refusal to cease such infringement, and its refusal to even meet with Impinj to address the dispute.

THE PARTIES

2. Impinj is a Delaware corporation with its principal place of business in Seattle, Washington.

3. Defendant NXP USA, Inc. ("NXP") is, on information and belief, a Delaware corporation, with its corporate headquarters in Austin, Texas. NXP is, upon information and belief, a subsidiary of NXP Semiconductors N.V. ("NXP Semiconductors"), a corporation headquartered in Eindhoven, Netherlands.

4. Venue is proper in this district under 28 U.S.C. § 1400(b) because NXP has committed acts of infringement and has a regular and established place of business in this district.

IMPINJ AND ITS PATENT RIGHTS

5. Impinj is a leading provider of RAIN RFID solutions, including hardware and software products that wirelessly connect everyday items to the internet. More specifically, Impinj sells a platform that includes endpoint integrated circuits ("ICs"), reader ICs, readers and gateways that enable wireless connectivity to everyday items, and software that delivers information about those connected items.

6. Impinj was founded in March 2000 based on research done at the California Institute of Technology by Carver Mead and Chris Diorio. Impinj has developed technology in connection with radio frequency identification, known as "RFID." Impinj has been instrumental in the development of what is now known as RAIN RFID, as well as to the formation of the RAIN RFID global alliance, which promotes the universal adoption of a certain type of RFID that uses ultra-high frequency ("UHF") radio waves and a communication protocol known as Gen2. From its inception, Impinj has been known as a leading innovator, particularly in the RAIN RFID space. The United

States Patent and Trademark Office has acknowledged many of Impinj's innovations, awarding Impinj more than 250 issued patents and allowed applications.

7. Impinj's RFID products include Monza RFID tag chips, which were the very first UHF Gen2 RFID tag chips. Impinj's current Monza R6 IC chip was the most advanced RFID chip available when introduced, and it has important features and/or functionality such as consistently accurate and high-quality data delivery, improved yield, auto-tuning to optimize readability for the environment and application, and other advanced features that have been recognized by the industry. Impinj also sells Indy reader chips, Speedway readers and gateways, and ItemSense Software.

NXP'S ACTS OF INFRINGEMENT

8. NXP makes and sells ICs that are used in RFID tags and compete with Impinj RAIN RFID ICs. NXP's products include UCODE 7 and UCODE 8 ICs, which are sold to various customers. The UCODE 8 IC was developed, on information and belief, by copying many of the patented inventions in Impinj's Monza R6 IC chip and in an attempt to mimic the quality and functionality of Impinj's Monza R6 IC.

9. After Impinj became aware of NXP's UCODE 8 ICs, it advised NXP Semiconductors, by letter dated August 11, 2017, that such ICs, and any associated RFID tags, were likely to infringe many U.S. patents owned by Impinj, which were listed by patent number.

10. In response, NXP by letter dated September 7, 2017, indicated it would need to see a "claim chart" before it would discuss the issues.

11. By letter dated September 14, 2017, Impinj suggested the parties meet in person, and provided a draft non-disclosure agreement to facilitate such discussions.

12. NXP indicated it would not enter into any non-disclosure agreement but reiterated its request for claim charts.

13. Since September 14, 2017, Impinj and NXP have exchanged correspondence relating to the dispute, including correspondence regarding infringement of Impinj's patents by NXP's UCODE 7 and UCODE 8 ICs. Impinj has provided NXP, among other things, claim charts detailing how NXP infringes the patents asserted below. Impinj has also requested, on multiple occasions, that the parties meet to try to resolve the issues.

14. For many of the asserted patents, NXP has not denied that the claims read on its products, but it asserted that it is the beneficiary of a license under the EPC™ Specification for RFID Air Interface Protocol for Communications at 860 MHz – 960 MHz ("Gen2 protocol"). Under that protocol, Impinj agreed to license patent claims that were "necessary" to practice the Gen2 protocol.

15. By claiming a license under the Gen2 protocol, NXP has admitted that it is practicing the claims of those patents.

16. None of the patent claims asserted below are necessary to practice the Gen2 protocol.

17. For other of the asserted patents, NXP has not denied that the claims read on its products but claimed that the patents are invalid.

18. NXP cannot establish that any of the asserted patents are invalid.

19. Despite numerous and repeated requests, NXP has refused to meet with Impinj to address its infringement of Impinj's patents.

20. Impinj was thus forced to file this lawsuit to protect its patent rights.

NXP'S INFRINGEMENT OF U.S. PATENT 10,002,266

21. Impinj owns U.S. Patent No. 10,002,266 ("the '266 Patent"), which is directed to an RFID IC that inventively reduces its clock frequency while tuning its impedance.

22. Claim 6 of the '266 Patent reads as follows:

> 6. A Radio Frequency Identification (RFID) integrated circuit (IC) requiring a minimum clock frequency to operate according to a protocol (MFOP), a sufficient power to tune a variable impedance (SPTT), and a sufficient power to operate according to the protocol (SPOI) greater than the SPTT, the IC comprising:
>
> a tuning circuit configured to tune the variable impedance during a tuning phase; and
>
> a processor block configured to:
>
> in the tuning phase:
>
> extract a first power at least equal to the SPTT from an RF wave; cause the tuning circuit to tune the variable impedance to increase power extraction from the RF wave; and

operate at a first clock frequency less than the MFOP while causing the tuning circuit to tune the variable impedance, wherein the IC is unable to communicate with an RFID reader according to the protocol while operating at the first clock frequency; and

in a protocol phase subsequent to the tuning phase: extract a second power at least equal to the SPOI from the RF wave;

operate at a second clock frequency greater than or equal to the MFOP; and

communicate with an RFID reader according to the protocol while operating at the second clock frequency.

23. Claim 8 of the '266 Patent reads as follows:

8. The IC of claim 6, wherein the processor block is further configured to:

initially operate in the tuning phase; and

subsequently operate in the protocol phase.

24. Claim 10 of the '266 Patent reads as follows:

10. The IC of claim 6, further comprising:

a first clock oscillator configured to provide the first clock frequency; and

a second clock oscillator configured to provide the second clock frequency.

25. NXP's UCODE 8 IC has each of the elements of claims 6, 8, and 10 of the '266 Patent, including the recited tuning circuit.

26. NXP has directly infringed the '266 Patent, including at least claims 8 and 10 of the '266 Patent, by making, importing, selling, and offering for sale UCODE 8 ICs.

27. NXP has continued its infringing activities despite knowledge of the '266 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

NXP'S INFRINGEMENT OF U.S. PATENT NO. 9,031,504

28. Impinj owns U.S. Patent No. 9,031,504 ("the '504 Patent"), which is directed to an inventive method of rejecting interference, to be performed by an RFID tag circuit.

29. Claim 1 of the '504 Patent reads as follows:

> 1. A method for a Radio Frequency Identification (RFID) tag circuit comprising:
>
> receiving a modulated wireless RF input signal;
>
> deriving a first digital output signal responsive to the modulated wireless RF input signal, wherein the first digital output signal comprises a sequence of digital pulses;
>
> generating artifact numbers by counting time durations of the digital pulses: and
>
> deriving a second digital output signal responsive to the first digital output signal at an interference rejection circuit of a RFID tag circuit by substantially removing digital pulses with artifact numbers less than a first low number while substantially retaining digital pulses with artifact numbers greater than the first low number, wherein the first low number corresponds to a first time duration threshold.

30. Claim 2 of the '504 Patent reads as follows:

> 2. The method of claim 1, further comprising determining the first time duration threshold from at least one of a frame-sync tari symbol encoded in the modulated wireless RF input signal, a data rate associated with the modulated wireless RF input signal, and a statistic of a characteristic of a received data packet.

31. Claim 7 of the '504 Patent reads as follows:

> 7. The method of claim 1, further comprising adjusting the first low number based on at least one aspect associated with the wireless RF input signal selected from at least one of a preamble, a received packet, a filtered output signal, a data rate, and an expected next packet.

32. NXP's UCODE 7 and UCODE 8 IC perform each of the steps of the methods recited in claims 1, 2, and 7 of the '504 Patent.

33. NXP has directly infringed the '504 Patent, including claims 1, 2 and 7 of the '504 Patent, by performing the recited methods through its use of its UCODE 7 and UCODE 8 ICs.

34. NXP has also indirectly infringed the '504 Patent, including claims 1, 2 and 7 of the '504 patent, under 35 U.S.C. §§ 271(b) and (c), by supplying its UCODE 7 and UCODE 8 ICs to

others. The UCODE 7 and UCODE 8 ICs have no substantial non-infringing use, and NXP has induced its customers to use the UCODE 7 and UCODE 8 ICs in a manner that leads the UCODE 7 and UCODE 8 ICs to perform the patented methods.

35. In the correspondence exchanged between the parties, NXP has not denied that it is practicing claims 1, 2, and 7 of the '504 Patent.

NXP has continued its infringing activities despite knowledge of the '504 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

NXP'S INFRINGEMENT OF U.S. PATENT NO. 9,633,302

36. Impinj owns U.S. Patent No. 9,633,302 ("the '302 Patent"), which is directed to an RFID IC with an inventive channel design.

37. Claim 1 of the '302 Patent reads as follows:

> 1. A Radio Frequency Identification (RFID) integrated circuit (IC) comprising:
>
> an IC substrate;
>
> a first antenna contact disposed on, and confined within a perimeter of, a surface of the IC substrate; and
>
> a second antenna contact disposed on, and confined within the perimeter of, the surface of the IC substrate; wherein:
>
> the first and second antenna contacts are separated by a channel having a first end, a second end opposite the first end, and a center between the first end and the second end;
>
> the channel spans a majority of a width of the IC substrate;
>
> a first transverse channel cross-section at the first end is substantially the same size as a second transverse channel cross-section at the second end and substantially larger than a third transverse channel cross-section at the center; and
>
> the channel is shaped to facilitate a fluid flow from the center to the first and second ends.

38. Claim 3 of the '302 Patent reads as follows:

> 3. The RFID IC of claim 1, wherein the channel has a non-convex shape.

39. Claim 4 of the '302 Patent reads as follows:

> 4. The RFID IC of claim 1, wherein the channel is substantially symmetric about at least one plane orthogonal to the surface of the IC substrate.

40. Claim 7 of the '302 Patent reads as follows:

> 7. The RFID IC of claim 1, wherein each of the antenna contacts includes:
>
> a raised nonconductive structure; and
>
> a conductive layer disposed on the raised nonconductive structure.

41. NXP's UCODE 7 and UCODE 8 ICs have each of the elements of claims 1, 3, 4 and 7 of the '302 Patent, including the recited channel design.

42. NXP has directly infringed the '302 Patent, including at least claims 1, 3, 4 and 7 of the '302 Patent, by making, importing, selling and offering for sale its UCODE 7 and UCODE 8 ICs.

43. NXP has continued its infringing activities despite knowledge of the '302 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

NXP'S INFRINGEMENT OF U.S. PATENT NO. 9,495,631

44. Impinj owns U.S. Patent No. 9,495,631 ("the '631 Patent"), which is directed to an RFID IC with an inventive contact layer structure for facilitating its placement on an inlay to make an RFID tag.

45. Claim 13 of the '631 Patent reads as follows:

> 13. A Radio Frequency Identification (RFID) integrated circuit (IC) comprising:
>
> a plurality of contact islands raised from a surface of the IC and separated from each other by at least one trench, the at least one trench spanning at least a width of an adjacent contact island, and the contact islands covering substantially an entire surface area of the IC except for the at least one trench, wherein each contact island includes:
>
> a nonconductive repassivation layer disposed on the surface of the IC;

a conductive contact layer disposed on and covering the re-passivation layer and confined within a perimeter of the IC; and

an electrical coupling between the contact layer and at least one of a rectifier, a modulator, and a demodulator in the IC.

46. Claim 14 of the ’631 Patent reads as follows:

14. The IC of claim 13, wherein the contact layer is metallic and is configured to protect the covered repassivation layer during etching.

47. Claim 15 of the ’631 Patent reads as follows:

15. The IC of claim 13, wherein the electrical coupling of at least one of the contact islands is through at least one of:

the repassivation layer of the respective contact island; and

a side contact disposed on a side of the respective contact island.

48. Claim 16 of the ’631 Patent reads as follows:

16. The IC of claim 13, wherein the contact layer is configured to couple to an antenna terminal on an inlay.

49. NXP’s UCODE 7 and UCODE 8 IC have each of the elements recited in claims 13, 14, 15, and 16 of the ’631 Patent, including the recited contact islands, trench and repassivation layer.

50. NXP has directly infringed the ’631 Patent, including at least claims 13, 14, 15 and 16 of the ’631 Patent, by making, importing, selling and offering for sale of its UCODE 7 and UCODE 8 ICs.

51. In the correspondence exchanged between the parties, NXP has not denied that it is practicing claims 13 and 15 of the ’631 Patent.

52. NXP has continued its infringing activities despite knowledge of the ’631 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

NXP'S INFRINGEMENT OF U.S. PATENT NO. 8,115,597

53. Impinj owns U.S. Patent No. 8,115,597 ("the '597 Patent"), which is directed to an IC for an RFID tag with an inventive circuit design for a power rectifier.

54. Claim 1 of the '597 Patent reads as follows:

> 1. A power rectifier for a Radio Frequency Identification tag circuit, comprising:
>
> a first antenna input node for receiving a first phase of an alternating RF wireless signal;
>
> a second antenna input node for receiving a second phase of the alternating RF wireless signal which is substantially opposite to the first phase;
>
> a plurality of serially coupled stages, at least one of the stages including
>
> a first synchronous element with a first beginning coupled to receive the second phase and a first ending, the first synchronous element including:
>
> a first transistor having an input terminal at the first beginning, an output terminal, and a gate coupled to receive the first phase; and
>
> a second transistor having an input terminal, an output terminal at the first ending, and a gate coupled to receive the second phase, in which the input terminal of the second transistor is connected to the output terminal of the first transistor at a first intermediate node so as to form a first charge-accumulating path between the first beginning and the first ending, and there is no charge-accumulating path between the first beginning and the first ending other than the first path; and
>
> a second synchronous element with a second beginning to receive a first phase and a second ending, the second synchronous element including:
>
> a third transistor having an input terminal at the second beginning, an output terminal, and a gate coupled to receive the second phase;
>
> a fourth transistor having an input terminal, an output terminal at the second ending, and a gate coupled to receive the first phase, in which the input terminal of the fourth transistor is connected to the output terminal of the third transistor at a second intermediate node so as to form a second charge-accumulating path between the second beginning and the second ending, and there is no charge-

accumulating path between the second beginning and the second ending other than the second path; and

in which the second beginning is coupled to the first ending.

55. Claim 12 of the '597 Patent reads as follows:

12. The rectifier of claim 1, in which the first and second intermediate nodes are coupled together, and are coupled to ground.

56. Claim 13 of the '597 Patent reads as follows:

13. A Radio Frequency Identification tag circuit, comprising:

a first antenna input node for receiving a first phase of an alternating RF wireless signal;

a second antenna input node for receiving a second phase of the alternating RF wireless signal which is substantially opposite to the first phase;

a plurality of serially coupled stages, at least one of the stages including:

a first synchronous element with a first beginning coupled to receive the second phase and a first ending, the first synchronous element including:

a first transistor having an input terminal at the first beginning, an output terminal, and a gate coupled to receive the first phase;

a second transistor having an input terminal, an output terminal at the first ending, and a gate coupled to receive the second phase, in which the input terminal of the second transistor is connected to the output terminal of the first transistor at a first intermediate node so as to form a first charge-accumulating path between the first beginning and the first ending, and there is no charge-accumulating path between the first beginning and the first ending other than the first path; and

a second synchronous element with a second beginning to receive the first phase and a second ending, the second synchronous element including:

a third transistor having an input terminal at the second beginning, an output terminal, and a gate coupled to receive the second phase;

a fourth transistor having an input terminal, an output terminal at the second ending, and a gate coupled to receive the first phase, in which the input terminal of the fourth transistor is connected to the output terminal of the third

transistor at a second intermediate node so as to form a second charge-accumulating path between the second beginning and the second ending, and there is no charge-accumulating path between the second beginning and the second ending other than the second path; and

in which the second beginning is coupled to the first ending.

57. Claim 15 of the '597 Patent reads as follows:

15. A rectifier for a Radio Frequency Identification tag circuit, comprising:

a first antenna input node for receiving a first phase of an alternating RF wireless signal;

a second antenna input node for receiving a second phase of the alternating RF wireless signal which is substantially opposite to the first phase;

a zeroth stage transistor having an input terminal connected to ground, an output terminal, and a gate coupled to receive the first phase;

a plurality of serially coupled stages, at least one of the stages including:

a first synchronous element with a first beginning coupled to receive the second phase and a first ending, the first synchronous element including:

a first transistor having an input terminal at the first beginning coupled to the output terminal of the zeroth stage transistor, an output terminal, and a gate coupled to receive the first phase;

a second transistor having an input terminal, an output terminal at the first ending, and a gate coupled to receive the second phase, in which the input terminal of the second transistor is connected to the output terminal of the first transistor at a first intermediate node so as to form a first charge-accumulating path between the first beginning and the first ending, and there is no charge-accumulating path between the first beginning and the first ending other than the first path; and

a second synchronous element with a second beginning to receive the first phase and a second ending, the second synchronous element including:

a third transistor having an input terminal at the second beginning, an output terminal, and a gate coupled to receive the second phase;

a fourth transistor having an input terminal, an output terminal at the second ending, and a gate coupled to receive the first phase, in which the input terminal of the fourth transistor is connected to the output terminal of the third transistor at a second intermediate node so as to form a second charge-accumulating path between the second beginning and the second ending, and there is no charge-accumulating path between the second beginning and the second ending other than the second path; and

in which the second beginning is coupled to the first ending.

58. NXP's UCODE 8 IC has each of the element of claims 1, 12, 13 and 15 of the '597 Patent, including the recited circuit structure.

59. NXP has directly infringed the '597 Patent, including at least claims 1, 12, 13 and 15 of the '597 Patent, by making, importing, selling and offering for sale its UCODE 8 ICs.

60. In the correspondence exchanged between the parties, NXP has not denied that it is practicing claim 13 of the '597 Patent.

61. On information and belief, NXP has continued its infringing activities despite knowledge of the '597 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

NXP'S INFRINGEMENT OF U.S. PATENT NO. 8,344,857

62. Impinj owns U.S. Patent No. 8,344,857 ("the '857 Patent"), which is directed to an inventive power rectifier design for an RFID tag.

63. Claim 1 of the '857 Patent reads as follows:

1. A rectifier for a Radio Frequency Identification tag, comprising:

a first antenna input,

a second antenna input,

first, second, third, and fourth capacitors,

a first transistor including an input terminal, an output terminal, and a gate, and

a second transistor of a type complementary to the first transistor and including

an input terminal, an output terminal, and a gate, wherein,

the input terminal of the first transistor is coupled to a beginning node,

the output terminal of the first transistor is coupled to an averaging node,

the input terminal of the second transistor is coupled to the averaging node,

the output terminal of the second transistor is coupled to an ending node,

the first antenna input is coupled to the gate of the first transistor and to the ending node,

the second antenna input is coupled to the gate of the second transistor and to the beginning node,

the first antenna input is coupled to the ending node via the first capacitor,

the second antenna input is coupled to the beginning node via the second capacitor,

the first antenna input is coupled to the gate of the first transistor via the third capacitor, and

the second antenna input is coupled to the gate of the second transistor via the fourth capacitor.

64. Claim 3 of the ’857 Patent reads as follows:

> 3. The rectifier of claim 1, further comprising a third transistor including an input terminal, an output terminal, and a gate, wherein the input terminal of the third transistor is coupled to a ground node, the output terminal of the third transistor is coupled to the beginning node, and the gate of the third transistor is coupled to the first antenna input.

65. Claim 4 of the ’857 Patent reads as follows:

> 4. The rectifier of claim 3, wherein the second and third transistors are of the same type.

66. Claim 6 of the ’857 Patent reads as follows:

> 6. A rectifier for a Radio Frequency Identification tag, comprising:
>
> a first antenna input,
>
> a second antenna input,

first, second, third, fourth, and fifth capacitors,

a first transistor including an input terminal, an output terminal, and a gate,

a second transistor of a complementary type to the first transistor and including

an input terminal, an output terminal, and a gate, and

a third transistor including an input terminal, an output terminal, and a gate, wherein:

the input terminal of the first transistor is coupled to a beginning node,

the output terminal of the first transistor is coupled to an averaging node,

the input terminal of the second transistor is coupled to the averaging node,

the output terminal of the second transistor is coupled to an ending node,

the input terminal of the third transistor is coupled to a ground node,

the output terminal of the third transistor is coupled to the beginning node,

the first antenna input is coupled to the gate of the first transistor, the gate of the third transistor, and the ending node,

the second antenna input is coupled to the gate of the second transistor and the beginning node,

the first antenna input is coupled to the ending node via the first capacitor,

the second antenna input is coupled to the beginning node via the second capacitor,

the first antenna input is coupled to the gate of the first transistor via the third capacitor and the gate of the third transistor via the fifth capacitor, and|

the second antenna input is coupled to the gate of the second transistor via the fourth capacitor.

67. Claim 7 of the ’857 Patent reads as follows:

7. The rectifier of claim 6, further comprising:

a fourth transistor including an input terminal, an output terminal, and a gate, and

a fifth transistor of a complementary type to the fourth transistor and the first transistor, and including an input terminal, an output terminal, and a gate, wherein:

the input terminal of the fourth transistor is coupled to the ending node,

the output terminal of the fourth transistor is coupled to a second averaging node,

the input terminal of the fifth transistor is coupled to the second averaging node,

the output terminal of the fifth transistor is coupled to a second ending node,

the first antenna input is further coupled to the gate of the fifth transistor, and

the second antenna input is further coupled to the gate of the fourth transistor and the second ending node.

68. Claim 8 of the ’857 Patent reads as follows:

8. The rectifier of claim 7, further comprising a sixth capacitor coupling the second antenna input to the second ending node.

69. Claim 9 of the ’857 Patent reads as follows:

9. The rectifier of claim 8, further comprising seventh and eight capacitors, wherein:

the first antenna input is coupled to the gate of the fifth transistor via the seventh capacitor, and

the second antenna input is coupled to the gate of the fourth transistor via the eighth capacitor.

70. NXP’s UCODE 7 and UCODE 8 ICs have each of the elements of claims 1, 3, 4, 6, 7, 8, and 9 of the ’857 Patent, including the recited circuit design.

71. NXP has directly infringed the ’857 Patent, including at least claims1, 4, 6 and 9 of the ’857 Patent, by making, importing, selling and offering for sale its UCODE 7 and UCODE 8 ICs.

72. In the correspondence exchanged between the parties, NXP has not denied that it is practicing claims 3, 4, 6, 7, 8, and 9 of the '857 Patent.

NXP has continued its infringing activities despite knowledge of the '857 Patent (including knowledge from correspondence with Impinj), and such infringement is egregious and willful.

REQUEST FOR RELIEF

WHEREFORE, Impinj requests the following relief:

(1) A preliminary and permanent injunction enjoining NXP and its officers, agents, servants, employees, attorneys and any other persons who are in active concert or participation with such persons, from making, selling, using, offering for sale or importing its UCODE 8 IC or any other IC that is not colorably different;

(2) For an award of damages, including lost profits, no less than a reasonable royalty under 35 U.S.C. § 284 arising from such infringement;

(3) For increased damages pursuant to 35 U.S.C. § 285 or as otherwise permitted by law;

(4) For an award of attorneys' fees and costs pursuant to 35 U.S.C. § 285 or as otherwise permitted by law; and

(5) For such other relief as the Court deems just and proper.

DATED: October 27, 2020.

By: */s/ Ramsey M. Al-Salam*

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